ELECTRICAL ENGG	5TH	NAME OF THE TEACHING FACULTY- NIHARIKA SETHY,	
SUB-DE & MP	No Of Days Per Week Class Alloted- 5	DECT(ETC.) 01.07.2024 TO 08.11.2024 NO OF WEEK – 15 WEEKS	
WEEK	CLASS DAY	THEORY	STATUS
1ST WEEK	1 ST day	Binary, Octal number systems and Hexadecimal	
	2 nd day 3 rd day 4 th day	number systems and	
		Compare with Decimal system.	1
	5th	Binary addition, subtraction, Multiplication and	
		Division.	
		1'scomplement and 2's complement numbers	
		for a binary number	
		Subtraction of binary numbers in 2's	
		complement method	
2 nd WEEK	1 ST day 2 nd day 3 rd day 4 th day 5th	Use of weighted and Un-weighted & codes Write Binary equivalent number for a, number in 8421 Excess-3 and Gray Code and vice-versa. Importance of parity Bit Logic Gates: AND,OR, NOT with truth table	
3 RD WEEK	1 ST day	NAND, NOR and EX-OR gates with truth table Realize AND, OR, NOT operations using	
	2 nd day	NAND, NOR gates	
	3 rd day 4 th day	Different postulates and De-Morgan's	
	5th	theorems.	
	Sili	Boolean algebra.	
		Use Of Boolean Algebra For Simplification Of	
		Logic Expression.	
4 TH WEEK	1 ST day	POS I i n	
	2 nd day	POS Logic Expression and SOP Logic Expression	
	3 rd day 4 th day 5th	1	
		Karnaugh Map	
		Karnaugh Map For 2,3,4 Variable,	
		Simplification Of SOP And POS	
	1 ST day	Logic Expression Using K-Map.	
	2 nd day 3 rd day 4 th day 5th	Give the concept of combinational logic circuits.	ř
5 TH WEEK		Half adder circuit, Full adder circuit and verify	
		its functionality using truth table	
		Half Subtractor and full subtractor explain its	
		operation with truth table	

		Multiplexer, De multiplexer	
		11,72	
			A
	. 72.		
	1 ST day 2 nd day	Encoder, Decoder	
	3 rd day	Give the idea of Sequential logic circuits.	
TIL	4 th day	State the necessity of clock and give the	
6 TH WEEK	5th	concept of level clocking and edge triggering	
		Clocked SR-flip flop with preset and	
		clear inputs	
	1 ST day	·	
	2 nd day	Construct level clocked JK flip flop using S-R	
	3 rd day 4 th day	flip-flop and explain with truth table	
	5th	JK flip flop using S-R flip-flop	
7 TH WEEK		Concept of race around condition	
		study of master slave JK flip flop	
it.	1 ST day	Give the truth tables of edge triggered D and T	
	2 nd day 3 rd day	flip flops and draw their symbols.	
	4 th day	Applications of flip flops.	
8 TH WEEK	5th		
		Introduction of counter. Define modulus of a	
		counter	
		4-bita synchronous counter and its timing	4
THE COLUMN		diagram.	
OTH WEEK	1 ST day 2 nd day	Asynchronous decade counter,	
	3 rd day	4-bit synchronous counter	
	4 th day	Distinguish between synchronous and	
	5 th day	asynchronous counters	
		State the need for a Register and list the four	
		types of registers.	1
72		Working of SISO, SIPO, PISO, PIPO Register	
		with truth table using flip flop.	
TH WEEK	1ST 4.	Industrial A. M.	1
DLK	1 ST day 2 nd day	Introduction to Microprocessors, Microcomputers	
	3 rd day	Architecture of Intel 8085 A Microprocessor	
	4 th day	and description of each block	
	5th day	Architecture of Intel 8085 A Microprocessor	
		and description of each block	
14.03		Pin diagram and description of 8085	
H WEEK	, ST.	Instruction set of 8085MP.	Eutro
EST MA	1 ST day 2 nd day	Subroutine. Stack, Stack pointer & stack top Interrupts	Extra classes needed to complete the
	3 rd day	Opcode & Operand,	syllabus
	4 th day	Differentiate between one byte, two byte &	
	5 th day		

12 TH WEEK 1 day 2 day 3 day 4 day 4 day 5 day 4 day 5 day 3 day 4 day 5 day 4 day 5 day 5 day 1 Si day 5 day 6 day 7 day 7 day 7 day 7 day 8 Seven segment LED display 8 Square wave generator 7 diffic light Controller 7 day 8 Doubt clerating classe 7 day 8 day 9 doubt clerating classe 7 day 8 day 9 doubt clerating classe 7 day 8 day 9 doubt clerating classe			Three byte instruction	
Jard day Jard d				
4 th day 5 th day Write, I/O read, I/O write. Timing Diagram for 8085 instruction Counter and time delay Simple assembly language programming of 8085 Simple assembly language programming of 8085 Simple assembly language programming of 8085 Basic Interfacing Concepts, Memory mapping & I/O mapping Functional block diagram of Intel 8255 5 th day Description of each block of Programmable peripheral Interface Intel 8255 Application using 8255 TH WEEK 1 ST day 2 nd day 3 rd day 3 rd day 3 rd day 3 rd day Traffic light Controller		2 nd day 3 rd day 4 th day 5 th day	three byte instruction with Addressing mode. Timing Diagram Machine Cycle, Instruction Cycle, T-State Fetch Cycle,	
HWEEK 1 ST day 2 nd day 3 rd day 4 th day 5 th day Description of each block of Programmable peripheral Interface Intel 8255 1 ST day 2 nd day 3 rd day 3 rd day 5 th day Seven segment LED display 5 th day 6 th day	a.T.H	4 th day 5 th day	write, I/O read, I/O write. Timing Diagram for 8085 instruction Counter and time delay Simple assembly language programming of 8085 Simple assembly language programming of	
TH WEEK 1 ST day Seven segment LED display Square wave generator Traffic light Controller Traffic light Controller Seven segment LED display Square wave generator Square wave generator Seven segment LED display Square wave generator Seven segment LED display Square wave generator Seven segment LED display Seven segment LED display Seven segment LED display Square wave generator Seven segment LED display Seven segment LED display Seven segment LED display Square wave generator Seven segment LED display Seven segment Seven	4 th WEEK	2 nd day 3 rd day 4 th day	Basic Interfacing Concepts, Memory mapping & I/O mapping Functional block diagram of Intel 8255 Description of each block of Programmable peripheral Interface Intel	
5 th day Semester question discussion	TH WEEK	2 nd day	Seven segment LED display Square wave generator Traffic light Controller Doubt cleraring class	

